

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT165

8-bit parallel-in/serial-out shift register

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit parallel-in/serial-out shift register

74HC/HCT165

FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs ($\overline{Q_7}$ and Q_7) available from the last stage. When the parallel load (\overline{PL}) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously.

When \overline{PL} is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input \overline{CE} should only take place while CP HIGH for predictable operation. Either the CP or the \overline{CE} should be HIGH before the LOW-to-HIGH transition of \overline{PL} to prevent shifting the data when \overline{PL} is activated.

APPLICATIONS

- Parallel-to-serial data conversion

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay CP to $Q_7, \overline{Q_7}$ \overline{PL} to $Q_7, \overline{Q_7}$ D_7 to $Q_7, \overline{Q_7}$ | C _L = 15 pF; V _{CC} = 5 V | 16 | 14 | ns |
| | | | 15 | 17 | ns |
| | | | 11 | 11 | ns |
| f _{max} | maximum clock frequency | | 56 | 48 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per package | notes 1 and 2 | 35 | 35 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

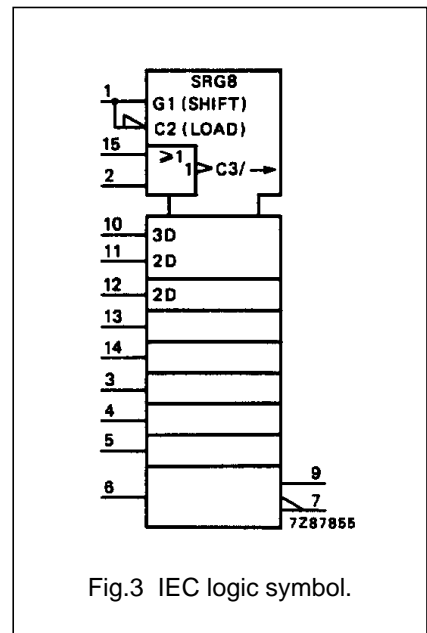
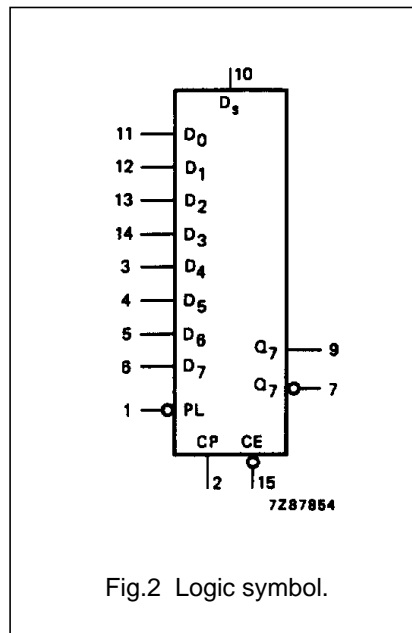
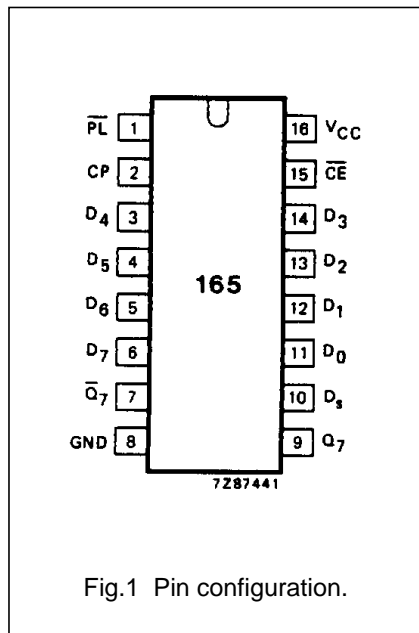
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-bit parallel-in/serial-out shift register

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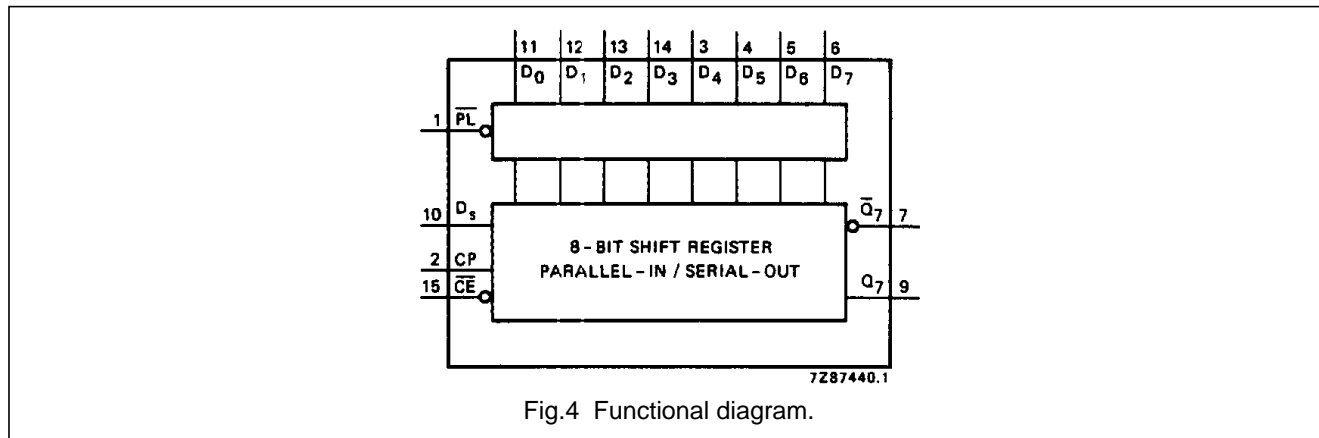
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------------------|------------------|---|
| 1 | \overline{PL} | asynchronous parallel load input (active LOW) |
| 7 | $\overline{Q_7}$ | complementary output from the last stage |
| 9 | Q_7 | serial output from the last stage |
| 2 | CP | clock input (LOW-to-HIGH edge-triggered) |
| 8 | GND | ground (0 V) |
| 10 | D_s | serial data input |
| 11, 12, 13, 14, 3, 4, 5, 6 | D_0 to D_7 | parallel data inputs |
| 15 | \overline{CE} | clock enable input (active LOW) |
| 16 | V_{CC} | positive supply voltage |



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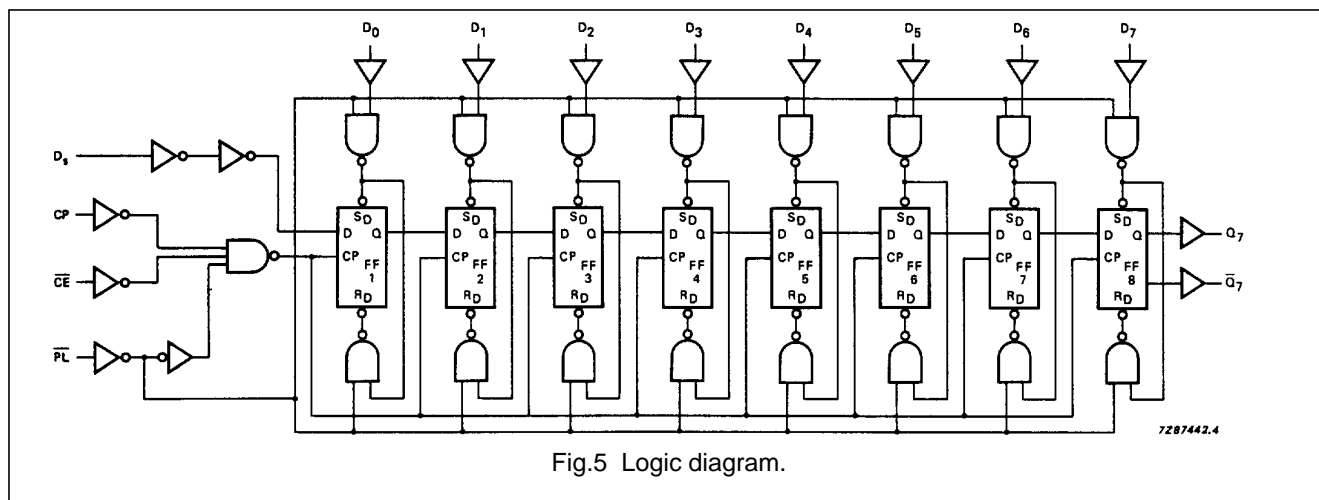


FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | Q _n REGISTERS | | OUTPUTS | |
|-------------------|-----------------|-----------------|----|----------------|--------------------------------|--------------------------|--------------------------------|----------------|------------------|
| | \overline{PL} | \overline{CE} | CP | D _s | D ₀ -D ₇ | Q ₀ | Q ₁ -Q ₆ | Q ₇ | $\overline{Q_7}$ |
| parallel load | L | X | X | X | L | L | L - L | L | H |
| | L | X | X | X | H | H | H - H | H | L |
| serial shift | H | L | ↑ | l | X | L | q ₀ -q ₅ | q ₆ | $\overline{q_6}$ |
| | H | L | ↑ | h | X | H | q ₀ -q ₅ | q ₆ | q ₆ |
| hold "do nothing" | H | H | X | X | X | q ₀ | q ₁ -q ₆ | q ₇ | q ₇ |

Note

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
 X = don't care
 ↑ = LOW-to-HIGH clock transition



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|--|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|-------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay \overline{CE} , CP to Q ₇ , $\overline{Q_7}$ | | 52 19 15 | 165 33 28 | | 205 41 35 | | 250 50 43 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay PL to Q ₇ , $\overline{Q_7}$ | | 50 18 14 | 165 33 28 | | 205 41 35 | | 250 50 43 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay D ₇ to Q ₇ , $\overline{Q_7}$ | | 36 13 10 | 120 24 20 | | 150 30 26 | | 180 36 31 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _w | clock pulse width HIGH or LOW | 80 16 14 | 17 6 5 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _w | parallel load pulse width; LOW | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{rem} | removal time PL to CP, \overline{CE} | 100 20 17 | 22 8 6 | | 125 25 21 | | 150 30 26 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{su} | set-up time D _s to CP, \overline{CE} | 80 16 14 | 11 4 3 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{su} | set-up time \overline{CE} to CP; CP to \overline{CE} | 80 16 14 | 17 6 5 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{su} | set-up time D _n to \overline{PL} | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |

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| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|------------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _h | hold time D _s to CP, $\overline{\text{CE}}$ D _n to $\overline{\text{PL}}$ | 5 | 6 | | 5 | | 5 | | ns | 2.0 | Fig.6 |
| | | 5 | 2 | | 5 | | 5 | | | 4.5 | |
| | | 5 | 2 | | 5 | | 5 | | | 6.0 | |
| t _h | hold time $\overline{\text{CE}}$ to CP CP to $\overline{\text{CE}}$ | 5 | -17 | | 5 | | 5 | | ns | 2.0 | Fig.6 |
| | | 5 | -6 | | 5 | | 5 | | | 4.5 | |
| | | 5 | -5 | | 5 | | 5 | | | 6.0 | |
| f _{max} | maximum clock pulse frequency | 6 | 17 | | 5 | | 4 | | MHz | 2.0 | Fig.6 |
| | | 30 | 51 | | 24 | | 20 | | | 4.5 | |
| | | 35 | 61 | | 28 | | 24 | | | 6.0 | |

8-bit parallel-in/serial-out shift register**74HC/HCT165**

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| D _n | 0.35 |
| D _s | 0.35 |
| CP | 0.65 |
| \overline{CE} | 0.65 |
| PL | 0.65 |

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AC CHARACTERISTICS FOR 74HCT

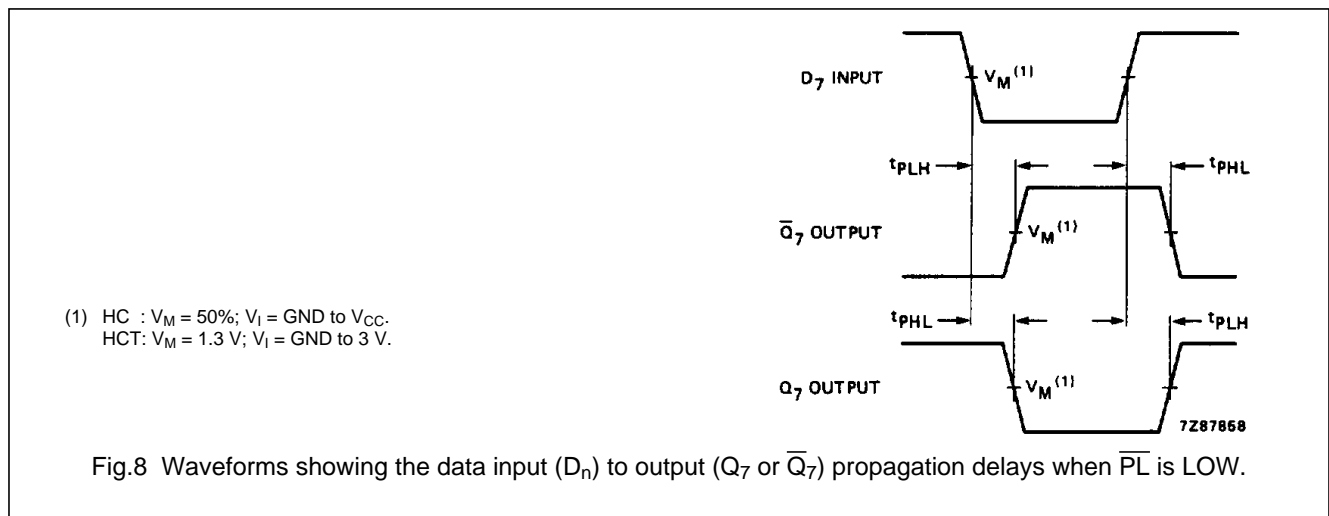
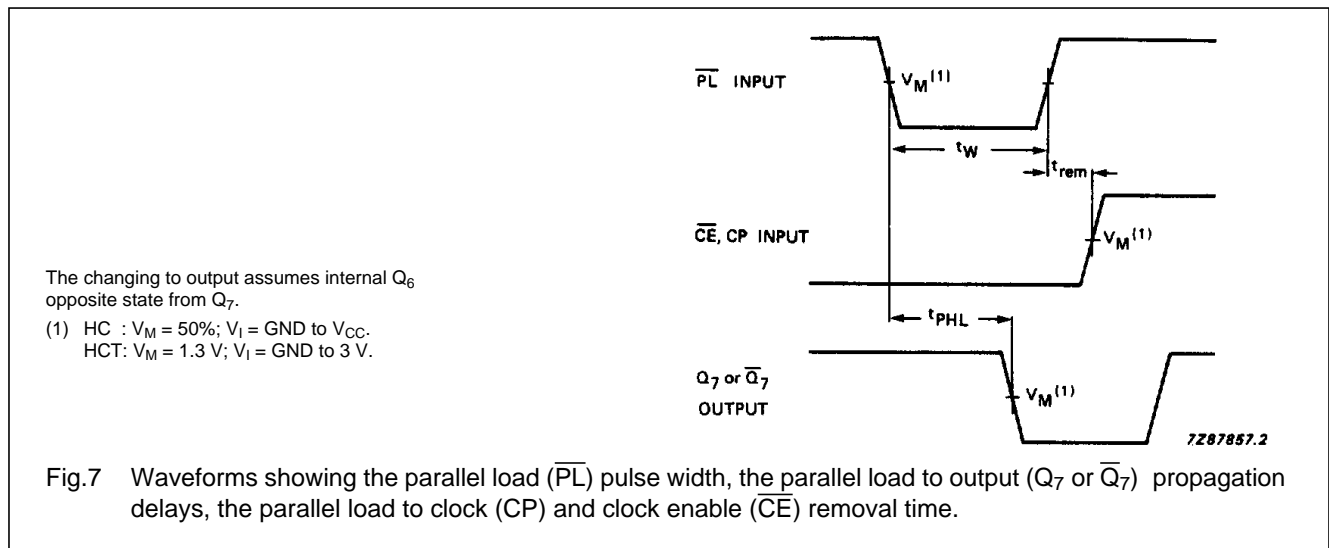
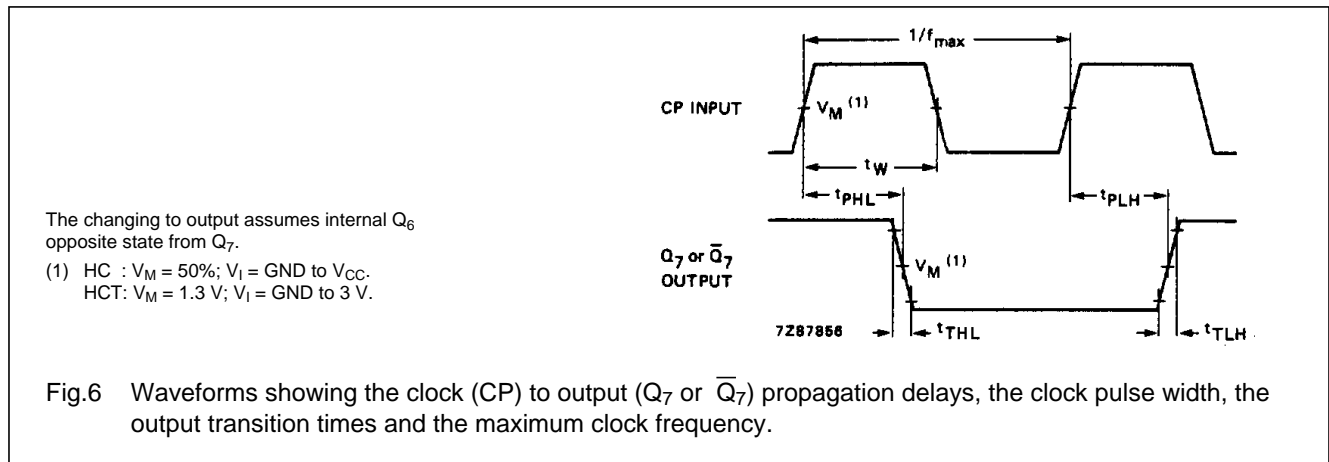
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------|--|----------------|------|------|------------|------|-------------|------|-----------------|-----------|-------|
| | | 74HCT | | | | | | | V_{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t_{PHL}/t_{PLH} | propagation delay \overline{CE} , CP to Q_7, \overline{Q}_7 | | 17 | 34 | | 43 | | 51 | ns | 4.5 | Fig.6 |
| t_{PHL}/t_{PLH} | propagation delay \overline{PL} to Q_7, \overline{Q}_7 | | 20 | 40 | | 50 | | 60 | ns | 4.5 | Fig.6 |
| t_{PHL}/t_{PLH} | propagation delay D_7 to Q_7, \overline{Q}_7 | | 14 | 28 | | 35 | | 42 | ns | 4.5 | Fig.6 |
| t_{THL}/t_{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |
| t_W | clock pulse width HIGH or LOW | 16 | 6 | | 20 | | 24 | | ns | 4.5 | Fig.6 |
| t_W | parallel load pulse width; LOW | 20 | 9 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| t_{rem} | removal time \overline{PL} to CP, \overline{CE} | 20 | 8 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| t_{su} | set-up time D_s to CP, \overline{CE} | 20 | 2 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| t_{su} | set-up time \overline{CE} to CP; CP to \overline{CE} | 20 | 7 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| t_{su} | set-up time D_n to \overline{PL} | 20 | 10 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| t_h | hold time D_s to CP, \overline{CE} ; D_n to \overline{PL} | 7 | -1 | | 9 | | 11 | | ns | 4.5 | Fig.6 |
| t_h | hold time \overline{CE} to CP, CP to \overline{CE} | 0 | -7 | | 0 | | 0 | | ns | 4.5 | Fig.6 |
| f_{max} | maximum clock pulse frequency | 26 | 44 | | 21 | | 17 | | MHz | 4.5 | Fig.6 |

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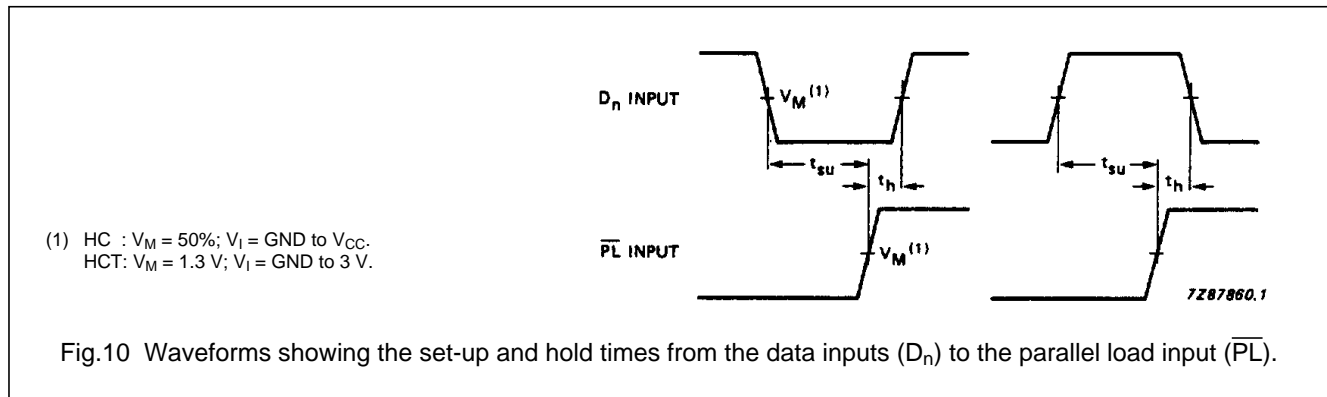
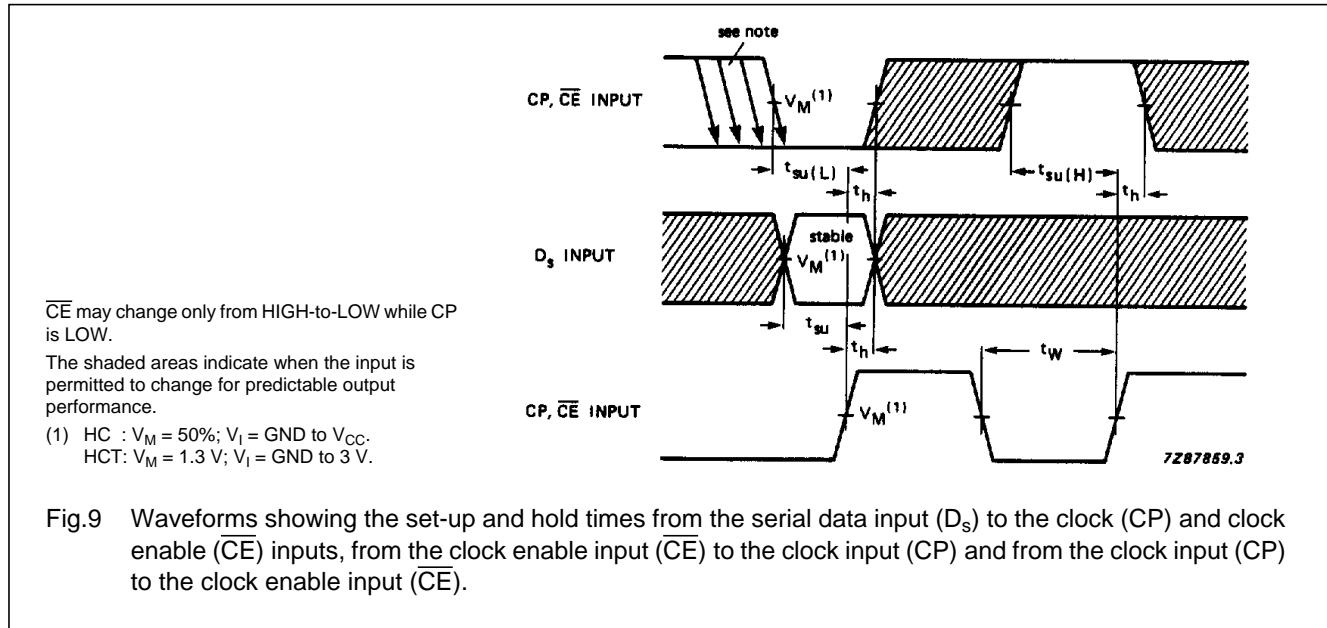
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AC WAVEFORMS



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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".